**Exercise: Inverter Sizing**

In order to drive a large capacitance (CL = 30 pF) from a minimum size inverter (with input capacitance Cin = 15fF), you decide to introduce a three-staged buffer as shown in Fig. 1. Assume that the propagation delay of a minimum size inverter driving another minimum size inverter is 90 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the three additional inverter stages that will minimize the propagation delay. Assume γ = 1.

